PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of	Docket No: Q77321
Hiroshi OKUMURA	
Appln. No.: 10/773,333	Group Art Unit: 3663
Confirmation No.: 8920	Examiner: Johannes P. MONDT
Filed: February 9, 2004	

For: THIN FILM TRANSISTOR SUBSTRATE AND METHOD OF MANUFACTURING THE SAME

SUBMISSION OF APPEAL BRIEF

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith please find an Appeal Brief. Since September 6, 2009 was a Sunday, and September 7, 2009 was a Federal Holiday, this Appeal Brief is timely filed on September 8, 2009. The USPTO is directed and authorized to charge the statutory fee of $540.00 and all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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Date: September 8, 2009

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APPEAL BRIEF UNDER 37 C.F.R. § 41.37

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 37 C.F.R. § 41.37, Appellant submits the following:

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I. REAL PARTY IN INTEREST

The real party in interest is NEC CORPORATION, by virtue of an assignment executed by Hiroshi Okumura on January 22, 2004, recorded on February 9, 2004 at Real 014977, Frame 0751.

II. RELATED APPEALS AND INTERFERENCES

To the knowledge and belief of Appellant, the Assignee, and the undersigned, there are no other appeals or interferences before the Board of Appeals and Interferences ("Board") that will directly affect or be affected by the Board's decision in the instant Appeal.

III. STATUS OF CLAIMS

Claims 14, 16 and 29-36 are all the claims pending in the application.

Claims 1-13, 15 and 17 have been cancelled without prejudice or disclaimer.

Claims 18-28 have been withdrawn from consideration based on Appellant's response to the restriction requirement in this application and, subsequently, non-elected claims 18-28 have been canceled without prejudice or disclaimer.

Claims 14, 16 and 29-36 presently stand rejected and are the subject of this Appeal.

IV. STATUS OF AMENDMENTS

The Advisory Action dated June 15, 2009 indicates that the Amendment Under 37 C.F.R. § 1.116 filed on May 26, 2009 has not been entered because the amendments to the specification set forth therein allegedly do not place the application in a better condition for Appeal.

There are no outstanding, non-entered amendments of the claims. The Appendix included with this Brief sets forth the claims involved in the Appeal and reflects the claims as presently presented in the application.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Appellant's invention relates generally to a thin film transistor substrate in which plural types of thin film transistors are formed on an insulating substrate and which provides circuit operation with high reliability. For example, by using polysilicon (poly-Si) thin film transistors, pixel switch elements and driver circuits can be formed on the same substrate in a liquid crystal device, organic EL display device, or the like, which is formed on a low-cost glass substrate. However, whereas a lower operation voltage is desired in the driver circuit for a lower power consumption, a higher voltage is required in pixel operation. Therefore, there is a need for a technique in which plural types of thin film transistors, with different operation voltages, are mixedly fabricated on a substrate so as to form a driver circuit including a power source booster circuit, a level shift circuit, or the like.

Illustrative embodiments of the claimed invention address the above needs in the art (and other needs) by providing a thin film transistor substrate in which the electric field is eased by a lightly doped drain structure in a low voltage driving thin film transistor and a structure in the high voltage driven thin film transistor. Accordingly, there can be formed a thin film transistor substrate including a circuit, which is constituted of plural kinds of thin film transistors, with a high throughput and which can be driven at high speed with low power consumption. Illustrative embodiments of the invention also provide a sub-gate structure in the high voltage driving thin film transistor that is excellent in output controllability at a low gate voltage, and therefore, is

appropriate for (among other things) a high withstand voltage thin film transistor used for a level shift circuit.

A. Identification of Independent Claims

The above discussion relates to illustrative embodiments of the invention, but also to the more generally expressed claim language of independent claim 29 below:

> A thin film transistor substrate comprising:
>
> an insulating substrate;
>
> a first thin film transistor formed above said insulating substrate, wherein said first thin film transistor comprises a first active layer formed above said insulating substrate, a first gate insulating film formed on said first active layer, and a first gate electrode formed on said first gate insulating film; and
>
> a second thin film transistor formed above said insulating substrate, wherein said second thin film transistor comprises a second active layer formed above said insulating substrate, a second gate insulating film formed on said second active layer, and a second gate electrode formed on said second gate insulating film,
>
> wherein said second gate insulating film comprises said first gate insulating film and a gate cover film formed above said first gate insulating film,
>
> wherein said second active layer has at least two impurity doping regions which overlap said second gate electrode,
>
> wherein said first active layer has at least two impurity doping regions formed in a self aligning manner with respect to said first gate electrode,

wherein said second thin film transistor further comprises a third gate electrode, wherein a gate length of said third gate electrode is shorter than a gate length of said second gate electrode, wherein said third gate electrode is formed between said second active layer and said second gate electrode and on the first gate insulating film,

wherein said impurity doping regions formed in a self-aligning manner are formed so as to overlap said first gate electrode by 0.1 μm or less, and

wherein said second active layer comprises a first channel region disposed directly below said second gate electrode, a second channel region disposed directly below said third gate electrode and an impurity doping region disposed between said first and second channel regions such that a portion of said impurity doping region is not directly below either said second gate electrode or said third gate electrode.

B. Mapping of Generally Expressed Claim Language of Independent Claim 29 to Specification by Page and Line Number

A thin film transistor substrate (*see e.g.,* lines 1-6 of new paragraph added before last full paragraph on page 18[1]; FIG. 11) comprising: an insulating substrate (*see e.g.,* page 11, lines 3-10; FIG. 11, element 101); a first thin film transistor (*see e.g.,* page 11, line 21 - page 12, line 6; FIG. 11, element 201) formed above said insulating substrate, wherein said first thin film transistor comprises a first active layer (*see e.g.,* page 11, lines 3-10; FIG. 11, element 102)

[1] New paragraph 0057.1 was added with the Amendment filed on November 21, 2008.

formed above said insulating substrate, a first gate insulating film (*see e.g.,* page 11, lines 3-10; FIG. 11, element 103) formed on said first active layer, and a first gate electrode (*see e.g.,* page 11, lines 3-10; FIG. 11, element 104) formed on said first gate insulating film; and a second thin film transistor (*see e.g.,* page 11, line 21 - page 12, line 6; lines 1-6 of new paragraph added before last full paragraph on page 18[2]; FIGS. 5(c) and 11, element 203 including first channel region 203a and second channel region 203b) formed above said insulating substrate, wherein said second thin film transistor comprises a second active layer (*see e.g.,* page 11, lines 3-10; FIG. 11, element 102) formed above said insulating substrate, a second gate insulating film (*see e.g.,* page 11, lines 3-10; FIG. 11, element 103) formed on said second active layer, and a second gate electrode (*see e.g.,* page 11, lines 11-20; FIG. 11, element 107) formed on said second gate insulating film, wherein said second gate insulating film comprises said first gate insulating film (*see e.g.,* page 11, lines 3-10; FIG. 11, element 103) and a gate cover film (*see e.g.,* page 11, lines 11-20; FIG. 11, element 106) formed above said first gate insulating film, wherein said second active layer has at least two impurity doping regions (*see e.g.,* page 14, lines 14-25; page 17, lines 13-19; page 17, line 20 - page 18, line 2; lines 1-6 of new paragraph added before last full paragraph on page 18[3]; FIG. 11, elements 105e and 105f) which overlap said second gate electrode, wherein said first active layer has at least two impurity doping regions (*see e.g.,* page 8, lines 4-12; page 11, lines 11-20; page 13, lines 1-11; page 16, lines 1-7; lines 1-6 of new

[2] New paragraph 0057.1 was added with the Amendment filed on November 21, 2008.

[3] New paragraph 0057.1 was added with the Amendment filed on November 21, 2008.

paragraph added before last full paragraph on page 18[4]; FIG. 11, elements 105a and 105b) formed in a self aligning manner with respect to said first gate electrode, wherein said second thin film transistor further comprises a third gate electrode (*see e.g.,* page 11, lines 3-10; page 15, lines 17-25; page 17, lines 13-19; page 17, line 20 - page 18, line 2; lines 1-6 of new paragraph added before last full paragraph on page 18[5]; FIG. 11, element 110), wherein a gate length of said third gate electrode is shorter than a gate length of said second gate electrode, wherein said third gate electrode is formed between said second active layer and said second gate electrode and on the first gate insulating film (*see e.g.,* FIG 11), wherein said impurity doping regions formed in a self-aligning manner are formed so as to overlap said first gate electrode by 0.1 μm or less, and wherein said second active layer comprises a first channel region (*see e.g.,* lines 1-6 of new paragraph added before last full paragraph on page 18[6]; FIG. 11, element 203a) disposed directly below said second gate electrode, a second channel region (*see e.g.,* lines 1-6 of new paragraph added before last full paragraph on page 18[7]; FIG. 11, element 203b) disposed directly below said third gate electrode and an impurity doping region disposed (*see e.g.,* page 17, lines 13-19; page 17, line 20 - page 18, line 2; lines 1-6 of new paragraph added before last full

[4] New paragraph 0057.1 was added with the Amendment filed on November 21, 2008.

[5] New paragraph 0057.1 was added with the Amendment filed on November 21, 2008.

[6] New paragraph 0057.1 was added with the Amendment filed on November 21, 2008.

[7] New paragraph 0057.1 was added with the Amendment filed on November 21, 2008.

paragraph on page 18[8]; FIG. 11, element 105f) between said first and second channel regions such that a portion of said impurity doping region is not directly below either said second gate electrode or said third gate electrode (*see e.g.,* FIG 11).

[8] New paragraph 0057.1 was added with the Amendment filed on November 21, 2008.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(1) Whether or not claims 29, 16 and 34-36 are unpatentable under 35 U.S.C. § 103(a) in view of Appellant's Admitted Prior Art (hereinafter "APA"), in view of JP 2003-017502A to Nakamura (hereinafter "Nakamura") and U.S. Patent No. 5,757,050 to Adler (hereinafter "Alder").

(2) Whether or not claim 14 is unpatentable under 35 U.S.C. § 103(a) in view of APA, Nakamura, Adler, and U.S. Patent No. 6,507,069 to Zhang (hereinafter "Zhang").

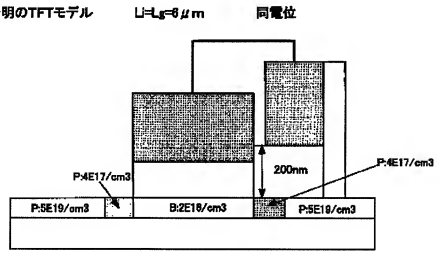
(3) Whether or not claim 30 is unpatentable under 35 U.S.C. § 103(a) in view of APA, Nakamura, Adler, and U.S. Patent No. 5,053,849 to Izawa et al. (hereinafter "Izawa").

(4) Whether or not claims 31 and 32 are unpatentable under 35 U.S.C. § 103(a) in view of APA, Nakamura, Adler, and U.S. Patent No. 6,048,795 to Numasawa et al. (hereinafter "Numasawa")

(5) Whether or not claim 33 is unpatentable under 35 U.S.C. § 103(a) in view of APA, Nakamura, Adler, and U.S. Patent No. 5,914,498 to Suzawa et al. (hereinafter "Suzawa").

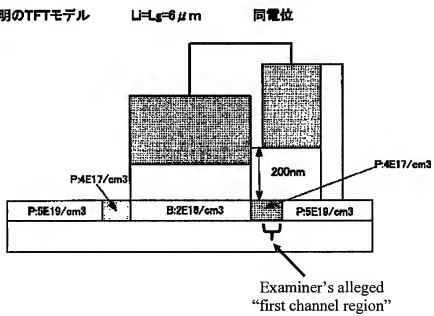
VII. ARGUMENT

There are clear errors in all of the Examiner's rejections *at least* because the cited references fail to teach or suggest the features of "wherein said second active layer comprises a first channel region disposed directly below said second gate electrode, a second channel region disposed directly below said third gate electrode and an impurity doping region disposed between said first and second channel regions such that a portion of said impurity doping region is not directly below either said second gate electrode or said third gate electrode," as recited in independent claim 29. The Examiner acknowledges that APA fails to teach or suggest these features but, nevertheless, alleges that the region marked P:5E19/cm^3 on the right side of Nakamura's Drawing 4A (reproduced below), or alternatively a sub-portion of the darkened region marked P:4E17/cm^3 disposed directly below the Nakamura's alleged second gate electrode, correspond to the recited "first channel region" and, thus, remedy the deficient teachings of APA.



The clear errors in the Examiner's rejections are explained in detail below.

First, during the interview conducted on June 9, 2009, the Examiner conceded that his allegations that Nakamura's region marked P:5E19/cm^3 corresponds to the claimed "channel region" were in error. Nevertheless, the Examiner maintained that a sub-portion of the region marked P:4E17/cm^3 in Nakamura disposed directly below the alleged second gate electrode still reads on the claimed "first channel region." By way of illustration, Nakamura's Drawing 4A has been reproduced below with an arrow and bracket transposed thereon to indicate the aspect of Nakamura relied upon by the Examiner as allegedly corresponding to the claimed "first channel region."



However, the Examiner's position relies on the conclusory statement[2] that there is nothing in the inherent properties of an lightly doped drain, or any other impurity doping region contiguous with a region that is at least during the ON state electrically connecting the source and the drain, that precludes it from functioning as a channel region. Accordingly, the Examiner interprets the "channel region" of claim 29 to require little more than an electron path between a source and a drain.

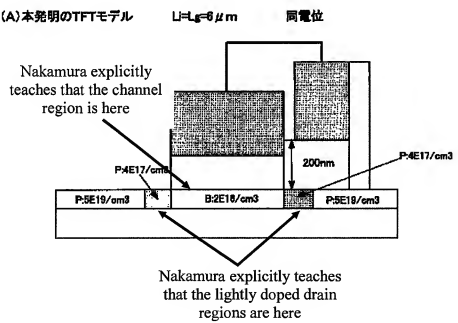
The Examiner's allegations in this regard are unsupported. The Examiner is required to give the claims their broadest reasonable interpretation (*see* MPEP §2111.01). One of ordinary skill in the art would not reasonably interpret the claimed "first channel region" to include any impurity doping region contiguous with a region that is at least during the ON state, as alleged by the Examiner. Quite to the contrary, the term "channel region" has a plain meaning to those of ordinary skill in the art that is clearly distinguishable from a lightly doped drain region like that taught in Nakamura.

Furthermore, contrary to the reasoning applied by the Examiner, one of ordinary skill in the art would have recognized that it is not necessary to use a transistor if it is always in an ON state. Thus, one of ordinary skill in the art would not have reasonably interpreted the claimed

[2] "Rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." KSR Int'l Co. v. Teleflex Inc., 127 S. Ct. 1727, 1741 (U.S. 2007).

"channel region" to include Nakamura's lightly doped drain region marked P:4E17/cm^3 or a sub-portion thereof for *at least* these reasons.

Second, Nakamura itself distinguishes between the channel region (i.e., the region marked B:2E16/cm^3) and the lightly doped drain region marked P:4E17/cm^3 and, therefore, Nakamura explicitly teaches away from the Examiner's proposed interpretation. For instance, as shown in Drawing 4A of Nakamura (reproduced below with annotations), the semiconductor layer consists of source and drain regions which are highly doped with n-type impurities (doped phosphorus (P) at a concentration of 5E19/cm^3 and these regions are referred to as "n+ regions"). Nakamura's semiconductor layer also consists of lightly doped drain regions which are lightly doped with n-type impurities (doped phosphorus (P) at a concentration of 4E17/cm^3 and these regions are referred to as "n- regions").



Moreover, as shown above, Nakamura's semiconductor layer consists of a channel region which is doped with p-type impurities (doped boron (B) at a concentration of $2E16/cm^3$ and this region is referred to as a "p region" or an "i (intrinsic) region").

As demonstrated by the above description of Drawing 4A, Nakamura's channel region (i.e., the region marked $B:2E16/cm^3$) is completely different from the lightly doped drain regions (i.e., the regions marked $P:4E17/cm^3$). For example, the channel regions have different dopant conductive types and different doping concentrations than the lightly doped drain regions. Indeed, the doping concentration of Nakamura's channel region differs from the doping concentration of Nakamura's lightly doped drain regions by several orders of magnitude. Therefore, no one skilled in the art would reasonably take the position that any of Nakamura's lightly doped drain regions correspond to a "channel region," as claimed.

Third, the 06/15/09 Advisory Action alleges that Appellant's arguments are not persuasive simply because the amount of doping of Nakamura's lightly doped drain regions is closer to that of the central channel region than it is to the conductivity of the source/drain regions. Appellant disagrees and submits that the Examiner has not provided any evidence in fact and/or reasoning in the official record to support such allegations.

Moreover, even assuming *arguendo* that the Examiner's allegations that the magnitude of the conductivities stand in the ratio of channel : lightly doped drain : source/drain = 1 : 20 : 2,500 *were* supported, such a ratio alone fails to demonstrate that one of ordinary skill in the art would have reasonably interpreted a "channel region," as claimed, to include Nakamura's lightly doped

drain region. Quite to the contrary, the Examiner's allegations actually support Appellant's position that Nakamura's channel region is completely different from the lightly doped drain regions disclosed therein since, if the Examiner's allegations *were* true, Nakamura would explicitly teach that the lightly doped drain regions therein exhibit completely different conductive properties than the channel region by a factor of 20 : 1 (i.e., several orders of magnitude).

Fourth, the Examiner's allegations that the relative horizontal extent of lightly doped drain doping regions, and particularly the feature of a non-overlapping portion of an lightly doped drain region, is an obvious matter of design choice because both with and without this feature, the performance of the thin film transistor substrate is qualified as useful, are unsupported by Nakamura. Nakamura in no way demonstrates that the feature of a non-overlapping portion of an lightly doped drain region is an obvious matter of design choice. In contrast, Nakamura clearly discloses that the electric field produced near the boundary of a channel formation field and an lightly doped drain field is eased. To obtain this effect, Nakamura teaches that the electrode 17 should be overlapped with gate electrode 13 as shown in all plan views, particularly Drawing 1A. That is, Nakamura teaches that the electrode 17 should be arranged over the boundary of the channel formation field and a lightly doped drain field. Indeed, Drawing 4A of Nakamura is nothing more than a schematic model. Therefore, Nakamura does not demonstrate that the feature of a non-overlapping portion of an lightly doped drain region is an obvious matter of design choice and cannot employ such a configuration.

In contrast to Nakamura, according to an illustrative embodiment shown in FIG. 11, the low voltage gate electrode 110 does not overlap lightly doped drain region 105f and the high voltage gate electrode 107 overlaps the lightly doped drain regions 105f and 105e. That is, the electric field is eased by a so-called lightly doped drain structure in the low voltage driving thin film transistor including low voltage gate electrode 110 and a so-called GOLD structure in the high voltage driven thin film transistor including high voltage gate electrode 107. Parasitic capacitance is more problematic in the low voltage driven thin film transistor than in the high voltage driving thin film transistor (*see* Specification, ¶26). Therefore, consistent with the claimed invention, there can be formed a thin film transistor substrate including a circuit which is constituted of plural kinds of thin film transistors with a high throughput and which can be driven at high speed with low power consumption.

Furthermore, claim 29 recites a sub-gate structure in the high voltage driving thin film transistor that is excellent in output controllability at a low gate voltage, and therefore, is appropriate for a high withstand voltage thin film transistor used for a level shift circuit (*see* Specification, ¶35). Such a sub-gate structure would not have been obvious in view of the cited references.

In view of the above clear errors, claim 29 is patentable over the cited references for *at least* the above reasons and the dependent claims 14, 16 and 30-36 are patentable *at least* by virtue of their dependency. Accordingly, Appellant respectfully requests that these rejections be overturned.

VIII. CONCLUSION

In view of the foregoing differences between appealed claims 14, 16 and 29-36 and Appellant's Admitted Prior Art, Nakamura, Adler, Zhang, Izawa, Numasawa and Suzawa, Appellant respectfully submits that the appealed claims are patentable over Appellant's Admitted Prior Art, Nakamura, Adler, Zhang, Izawa, Numasawa and Suzawa, and any combination thereof.

The USPTO is directed and authorized to charge the statutory fee (37 C.F.R. §41.37(a) and 1.17(c)) and all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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CLAIMS APPENDIX

CLAIMS 14, 16 and 29-36 ON APPEAL:

14. The thin film transistor substrate according to claim 29,

wherein at least one of said impurity doping regions formed in a self-aligning manner with respect to said first gate electrode includes an LDD structure.

16. The thin film transistor substrate according to claim 29,

wherein at least one of impurity doping regions which overlap said second gate electrode includes an LDD structure.

29. A thin film transistor substrate comprising:

an insulating substrate;

a first thin film transistor formed above said insulating substrate, wherein said first thin film transistor comprises a first active layer formed above said insulating substrate, a first gate insulating film formed on said first active layer, and a first gate electrode formed on said first gate insulating film; and

a second thin film transistor formed above said insulating substrate, wherein said second thin film transistor comprises a second active layer formed above said insulating substrate, a

second gate insulating film formed on said second active layer, and a second gate electrode formed on said second gate insulating film,

wherein said second gate insulating film comprises said first gate insulating film and a gate cover film formed above said first gate insulating film,

wherein said second active layer has at least two impurity doping regions which overlap said second gate electrode,

wherein said first active layer has at least two impurity doping regions formed in a self aligning manner with respect to said first gate electrode,

wherein said second thin film transistor further comprises a third gate electrode, wherein a gate length of said third gate electrode is shorter than a gate length of said second gate electrode, wherein said third gate electrode is formed between said second active layer and said second gate electrode and on the first gate insulating film,

wherein said impurity doping regions formed in a self-aligning manner are formed so as to overlap said first gate electrode by 0.1 μm or less, and

wherein said second active layer comprises a first channel region disposed directly below said second gate electrode, a second channel region disposed directly below said third gate electrode and an impurity doping region disposed between said first and second channel regions such that a portion of said impurity doping region is not directly below either said second gate electrode or said third gate electrode.

30. The thin film transistor substrate according to claim 29 wherein said impurity doping regions which overlap said second gate electrode are formed so as to overlap said second gate electrode by 2.0 μm or less.

31. The thin film transistor substrate according to claim 29 wherein said third gate electrode comprises a two-layer structure including a semiconductor layer and a metal or a metal silicide layer.

32. The thin film transistor substrate according to claim 29,

wherein said second gate electrode comprises a semiconductor layer.

33. The thin film transistor substrate according to claim 29,

wherein said third gate electrode is formed of the same material as said first gate electrode, and

wherein said third gate electrode has the same thickness as said first gate electrode.

34. The thin film transistor substrate according to claim 29,

wherein said first gate electrode, said second gate electrode and said third gate electrode are formed under wires which connect to said impurity doping regions.

35. The thin film transistor substrate according to claim 29, wherein the impurity doping region existing between the second gate electrode and the third gate electrode is an LDD region.

36. The thin film transistor substrate according to claim 29, wherein said first channel region, said second channel region and said impurity doping region are configured in a plane configuration.

EVIDENCE APPENDIX

This Appendix is not applicable to this Appeal.

RELATED PROCEEDINGS APPENDIX

This Appendix is not applicable to this Appeal.